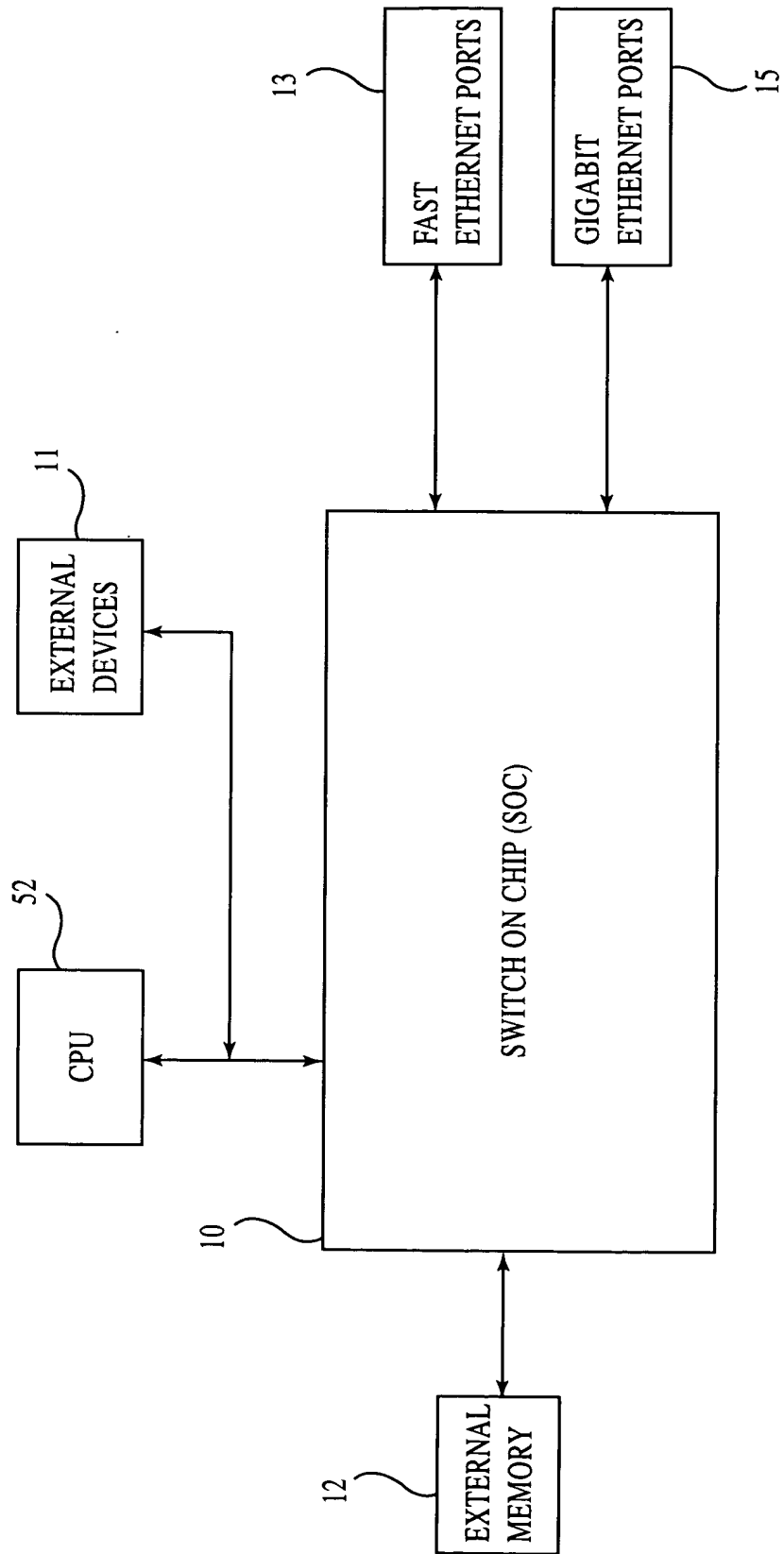


Fig.1



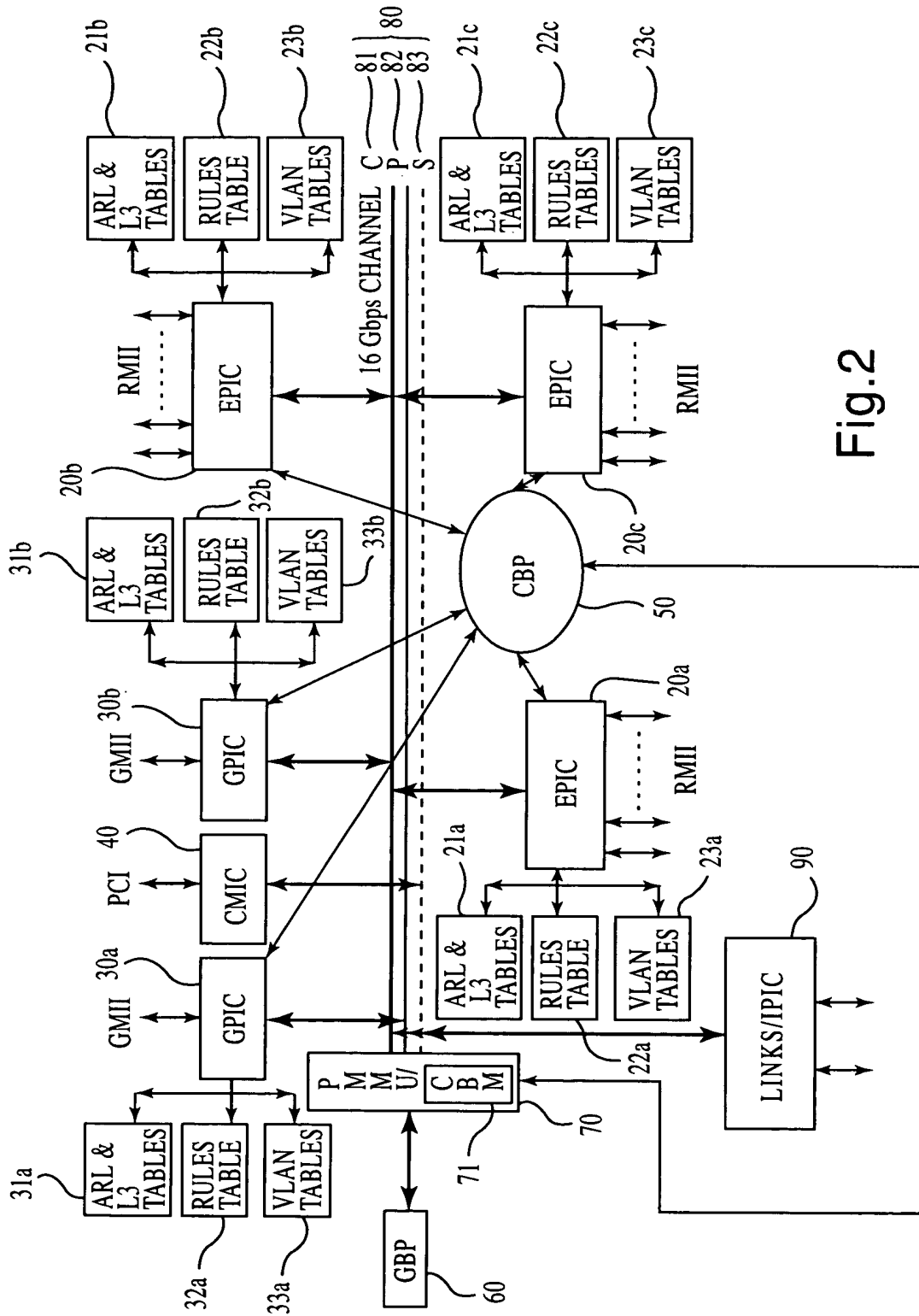


Fig.2

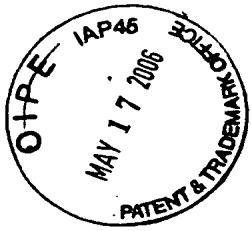
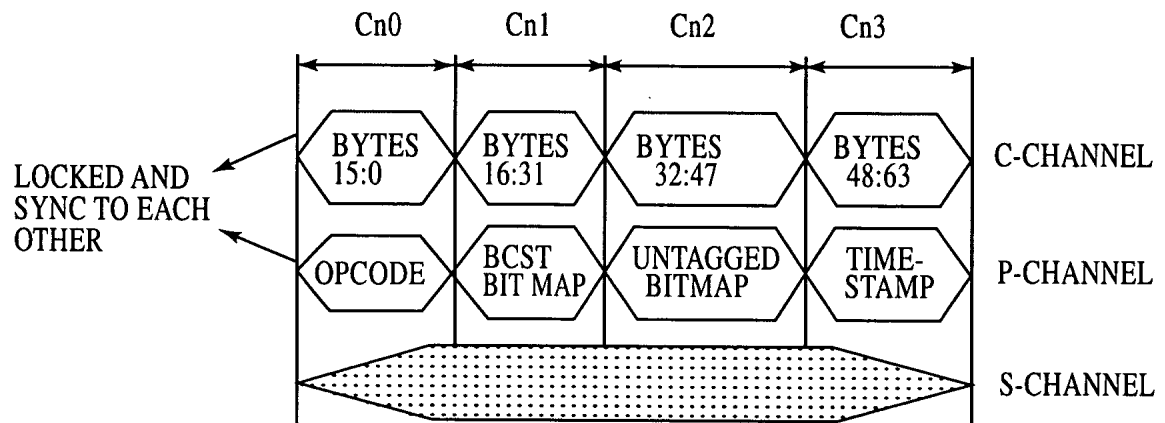


Fig.3



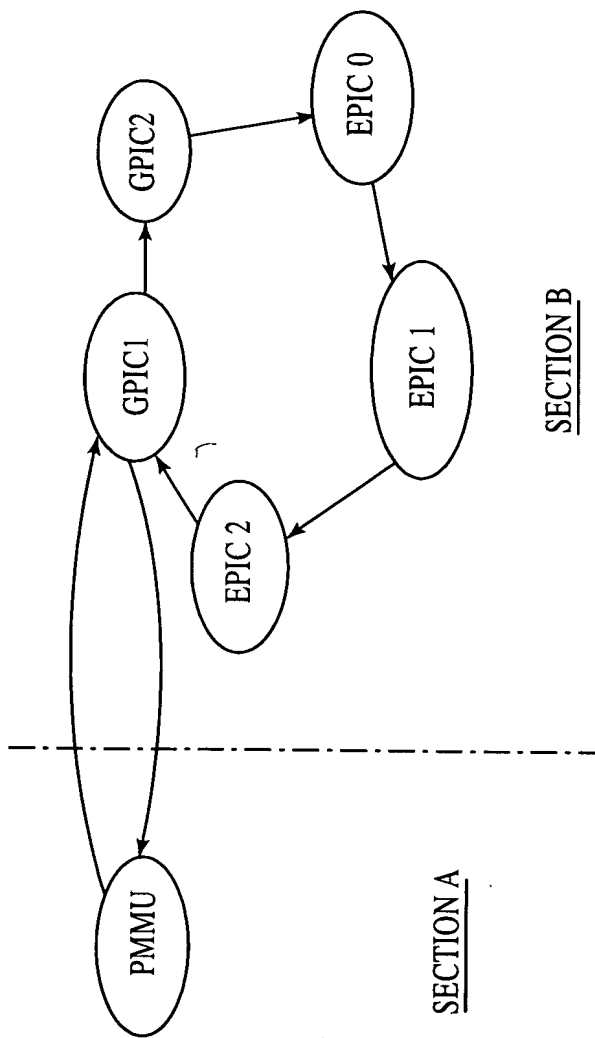
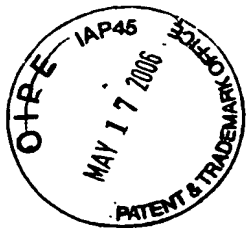


Fig.4a

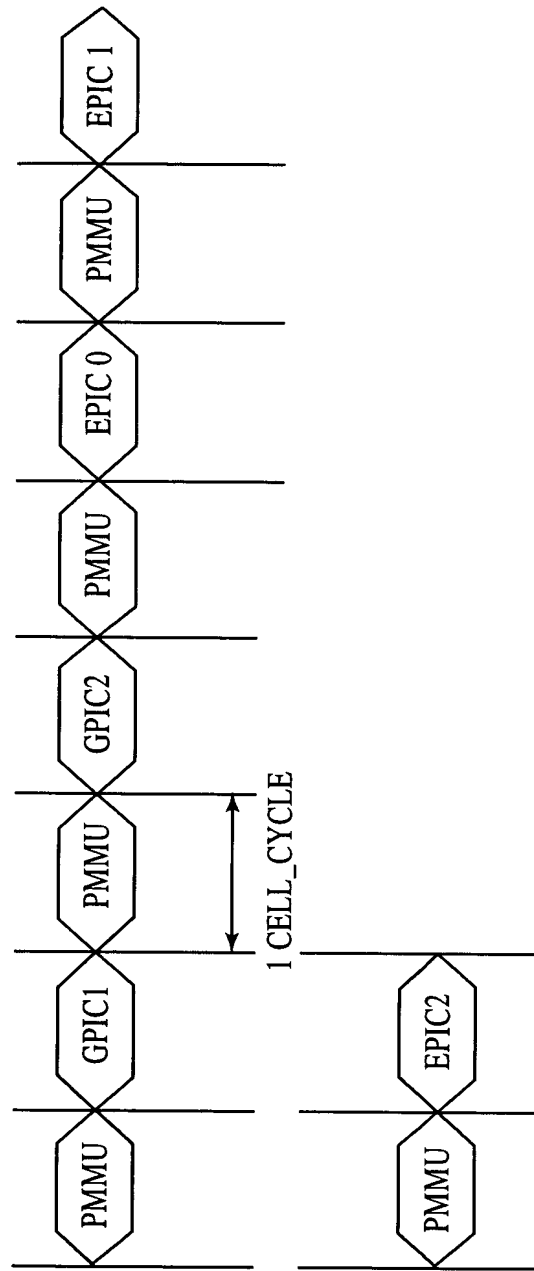


Fig.4b

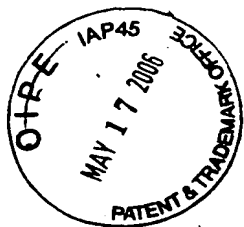


Fig. 5

PROTOCOL CHANNEL MESSAGES

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
OP CODE	I	RESERVED	NXT CELL	SRC DEST PORT				COS	J	S	E	CR C	P	O	LEN
	I			P	X										

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
RESERVED															
BC/MC PORTBITMAP															

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
U	RES	UNTAGGED PORTBITMAP/SRC PORT NUMBER (BIT0..5)													

CPU OPCODES										TIMESTAMP					
30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0

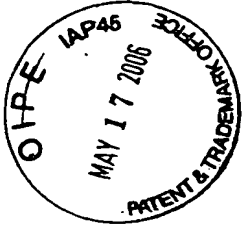
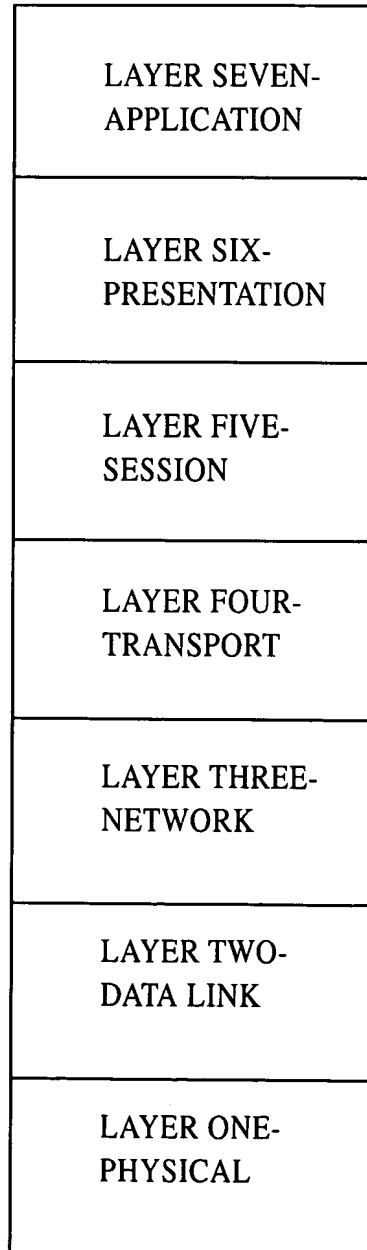


Fig.7
PRIOR ART



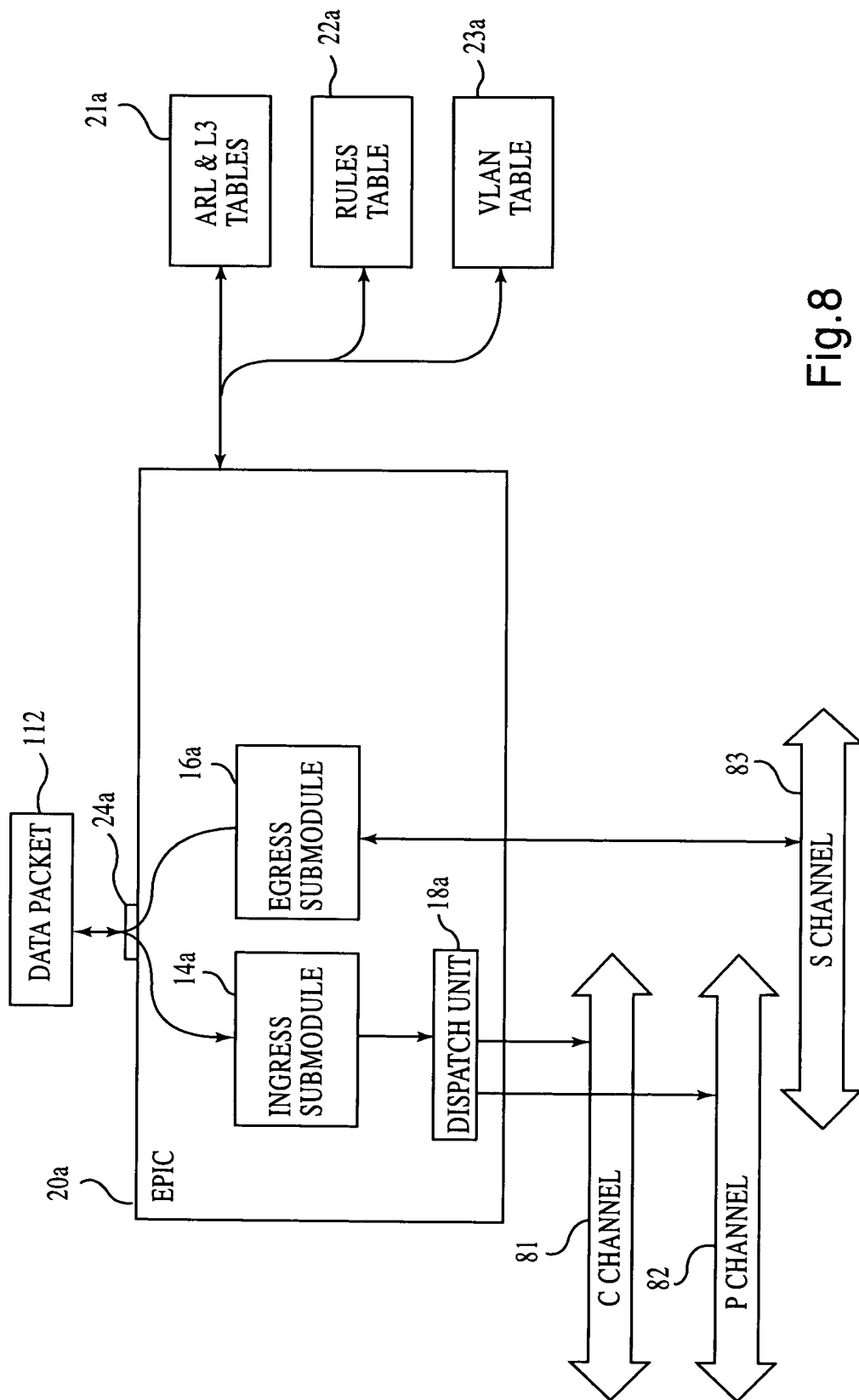


Fig.8

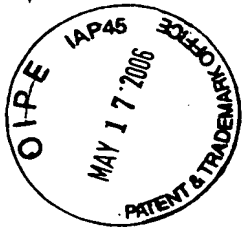
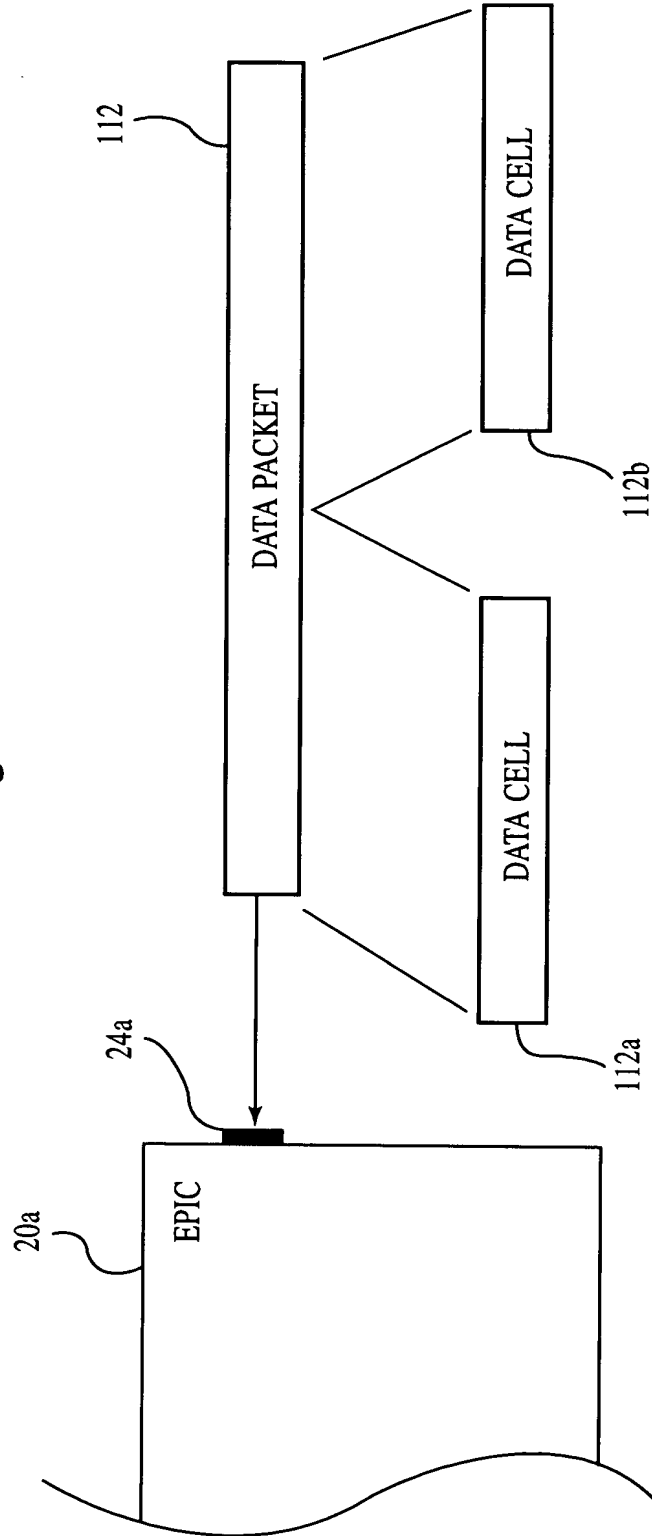


Fig.9



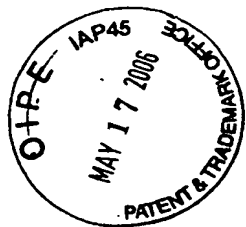
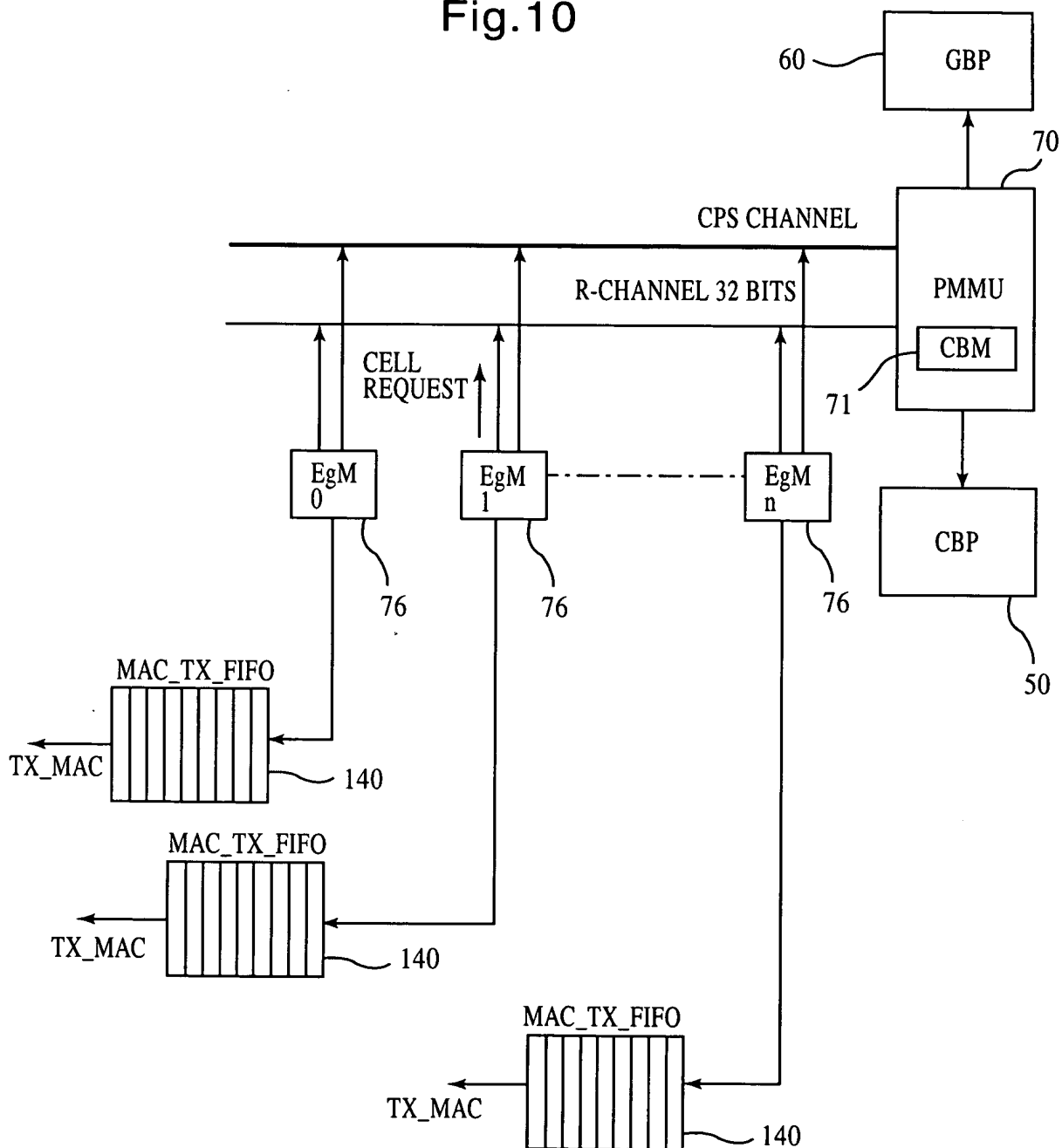


Fig.10



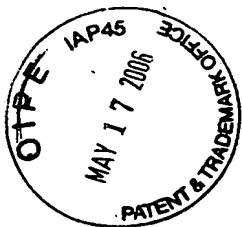


Fig.11

LINE 0 →	FC LC BC/MC Cpy_cnt (5b) Cell_length (7b) CRC (2b) NC_header (16b) Src Count (6) IPX IP Time_Stamp (14b) O bits (2b) P NextCellLen(2b) CpuOpcode(4b) Cell_data (0-9B)
LINE 1 →	Cell_data (10-27) Bytes
LINE 2 →	Cell_data (28-45) Bytes
LINE 3 →	Cell_data (46-63) Bytes

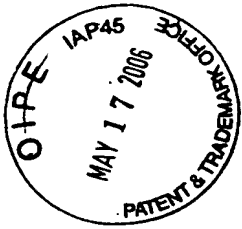
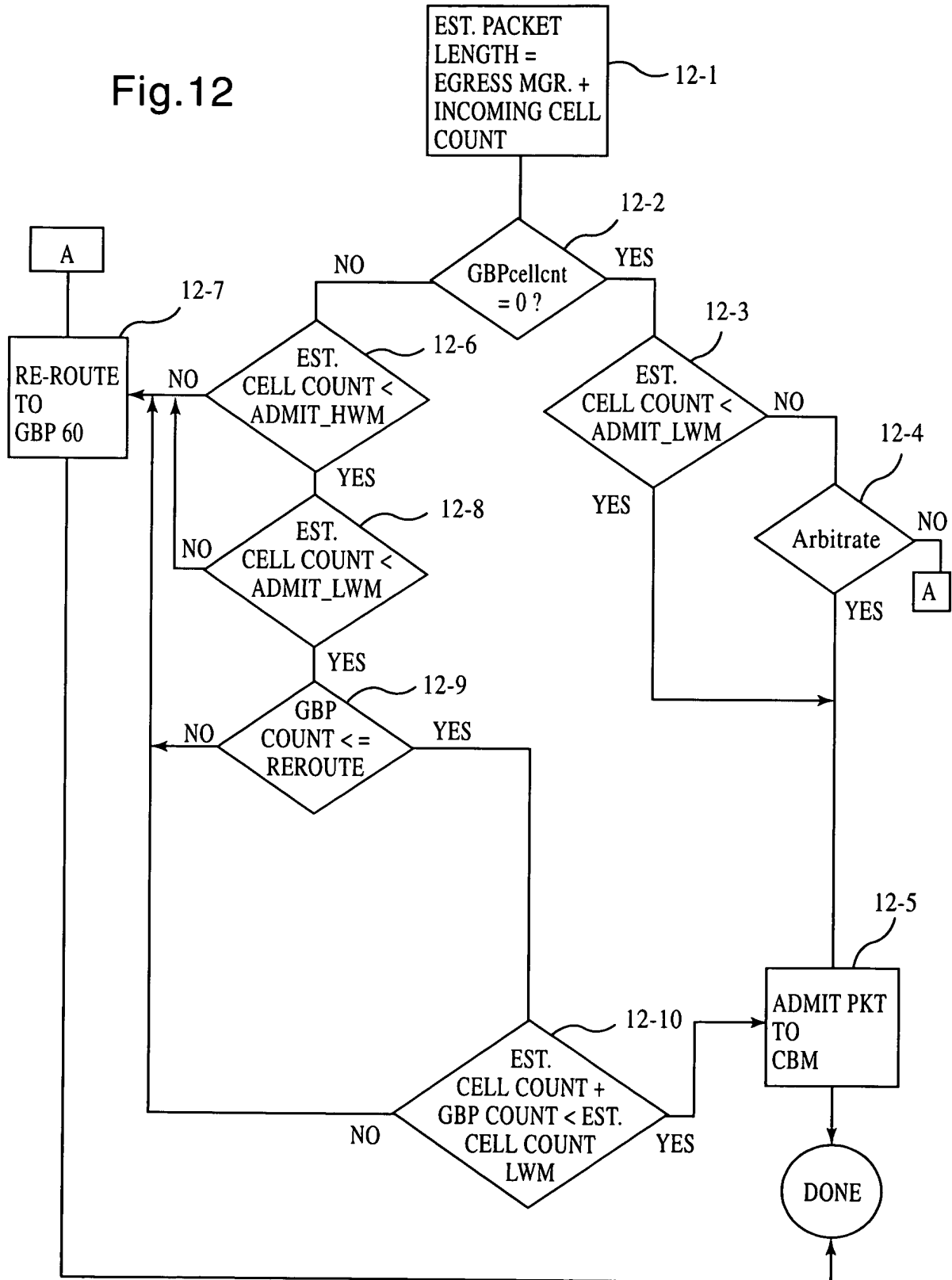


Fig.12



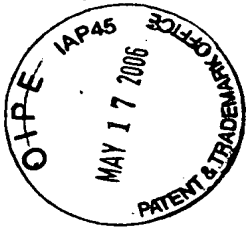
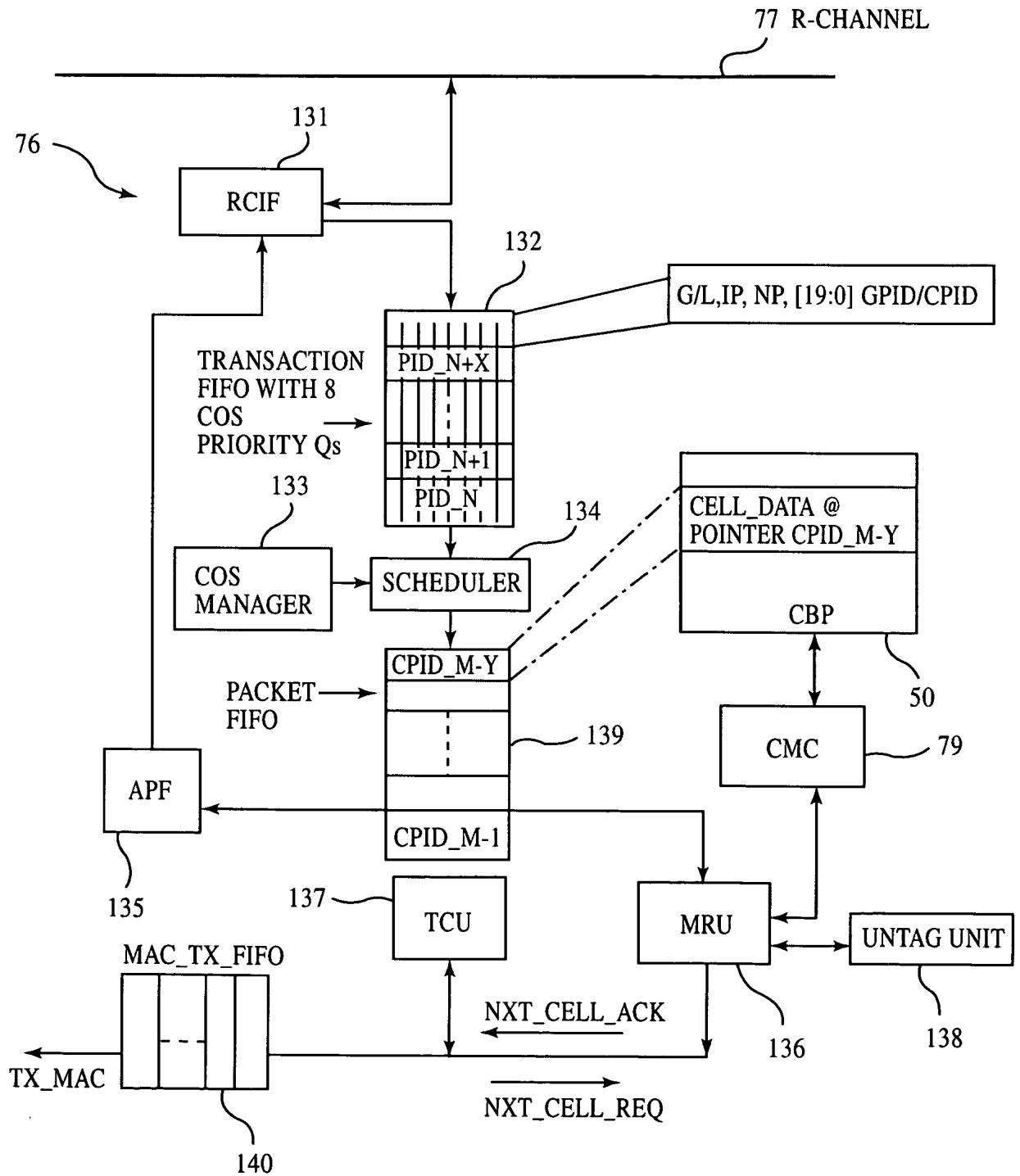


Fig.13



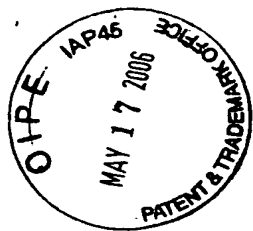
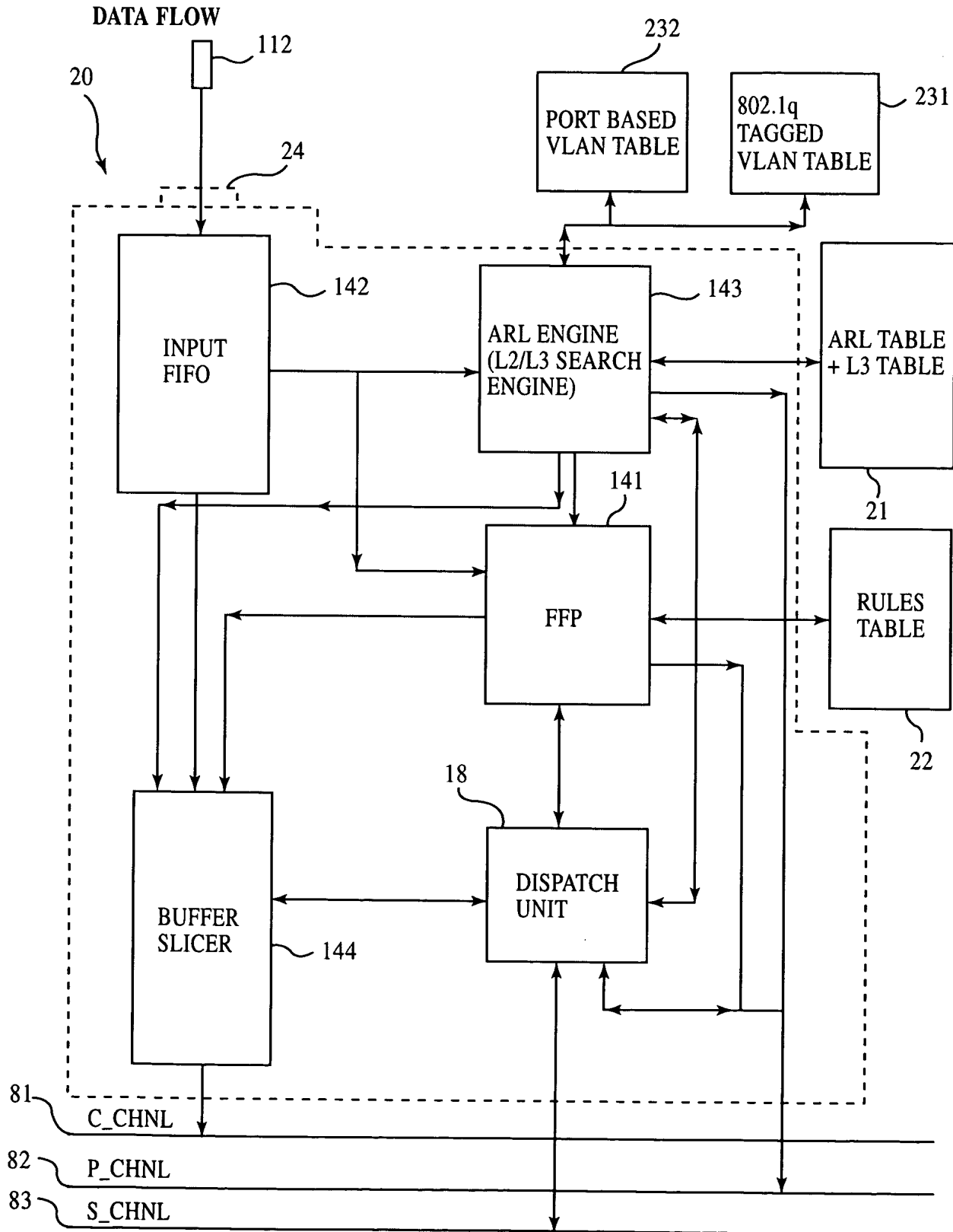


Fig.14



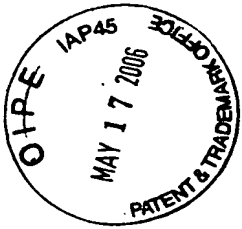
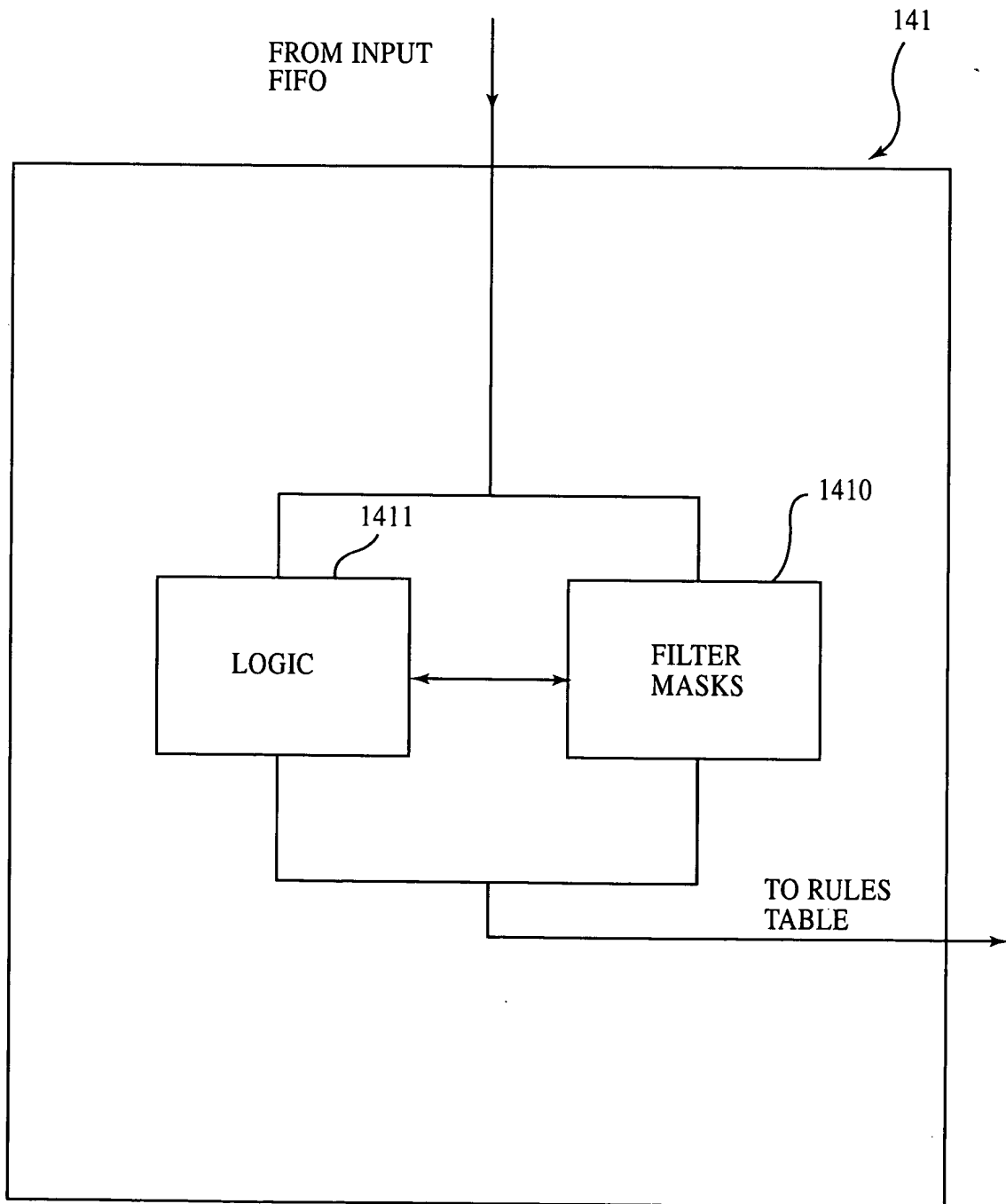


Fig.15



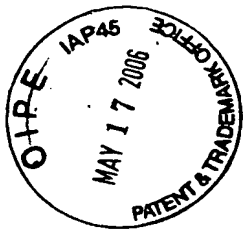
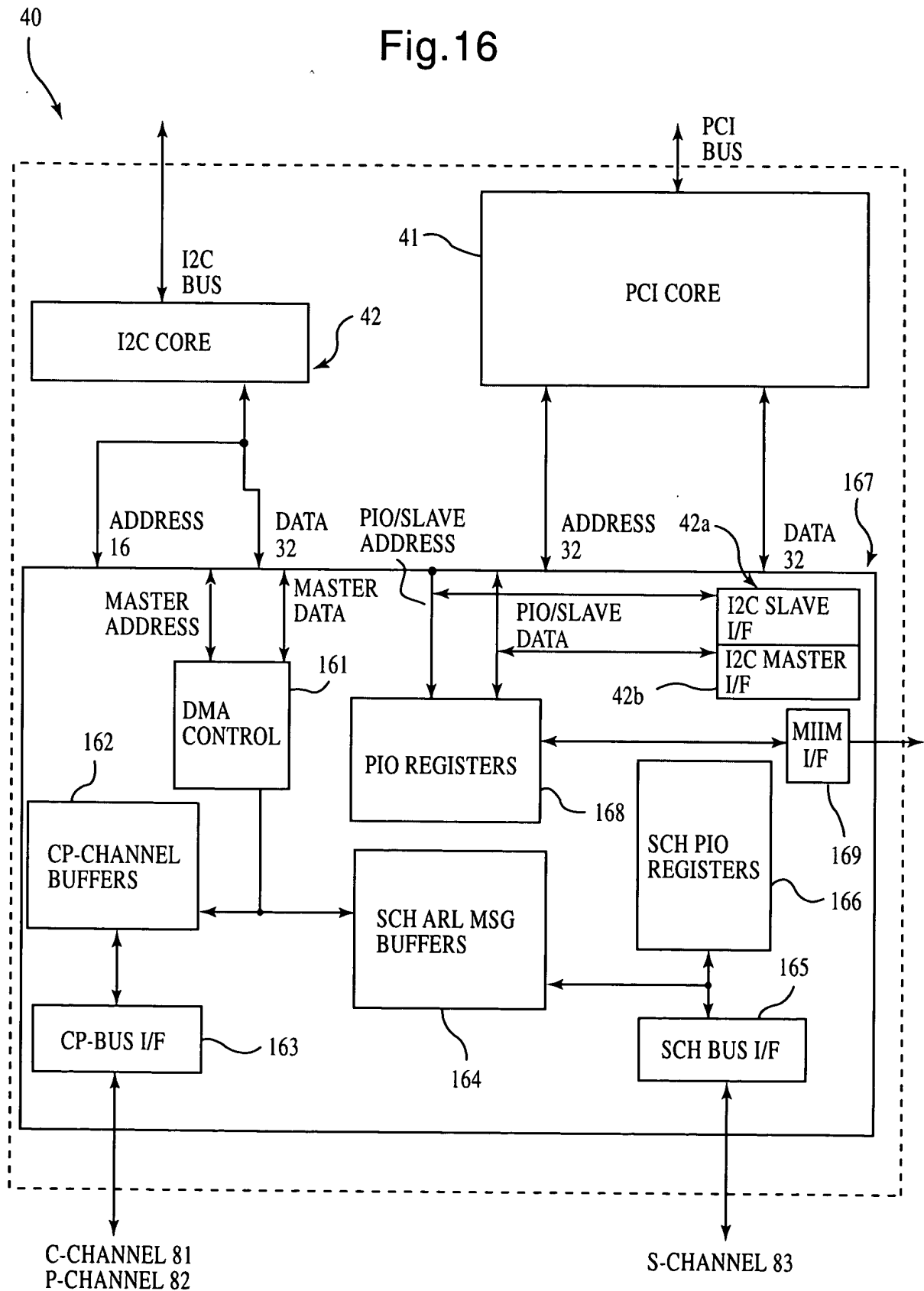


Fig.16



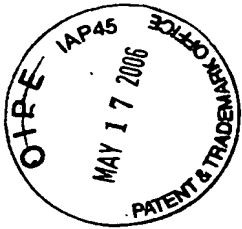
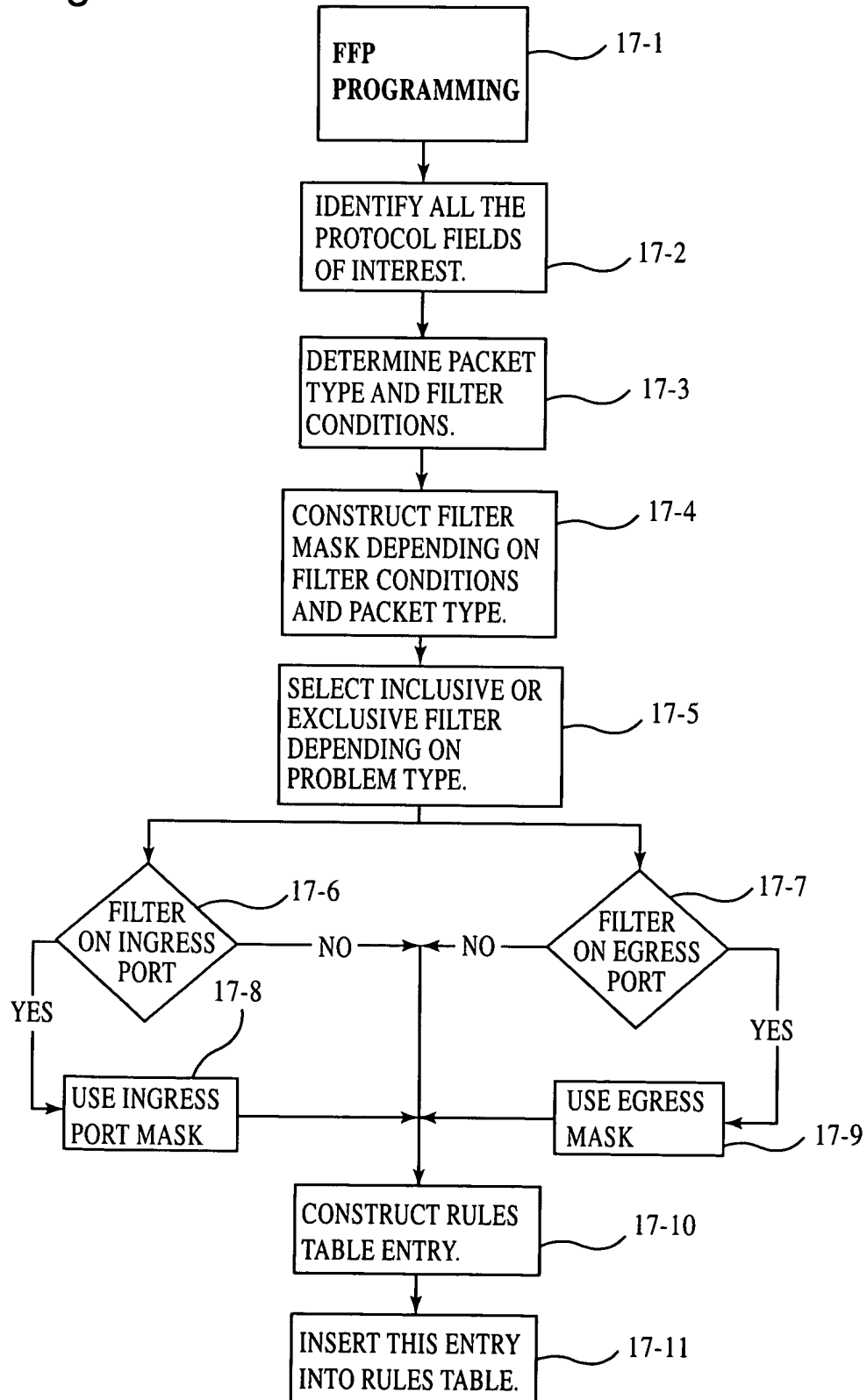
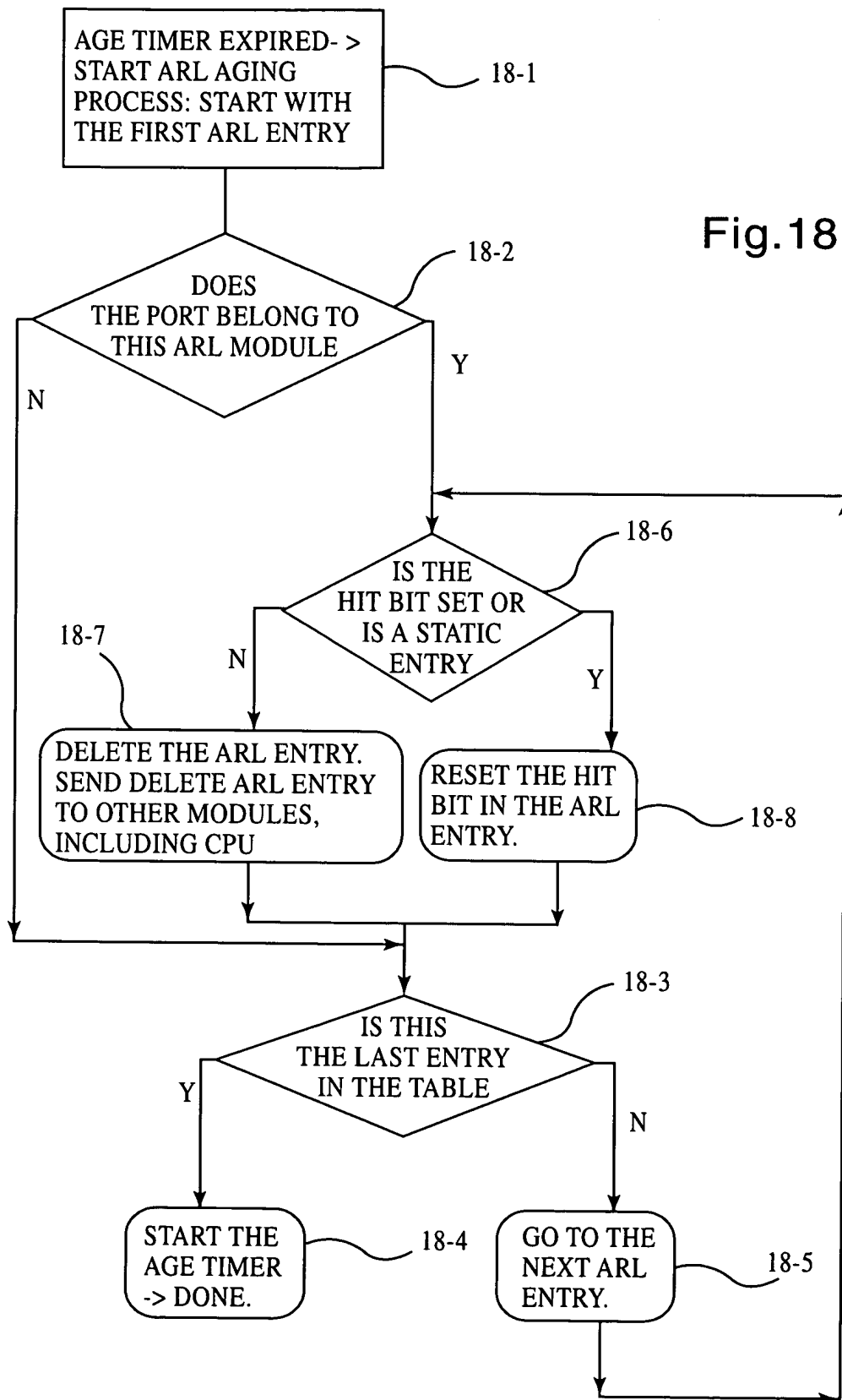
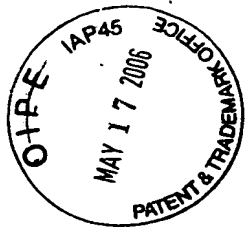


Fig.17

FFP PROGRAMMING FLOW CHART





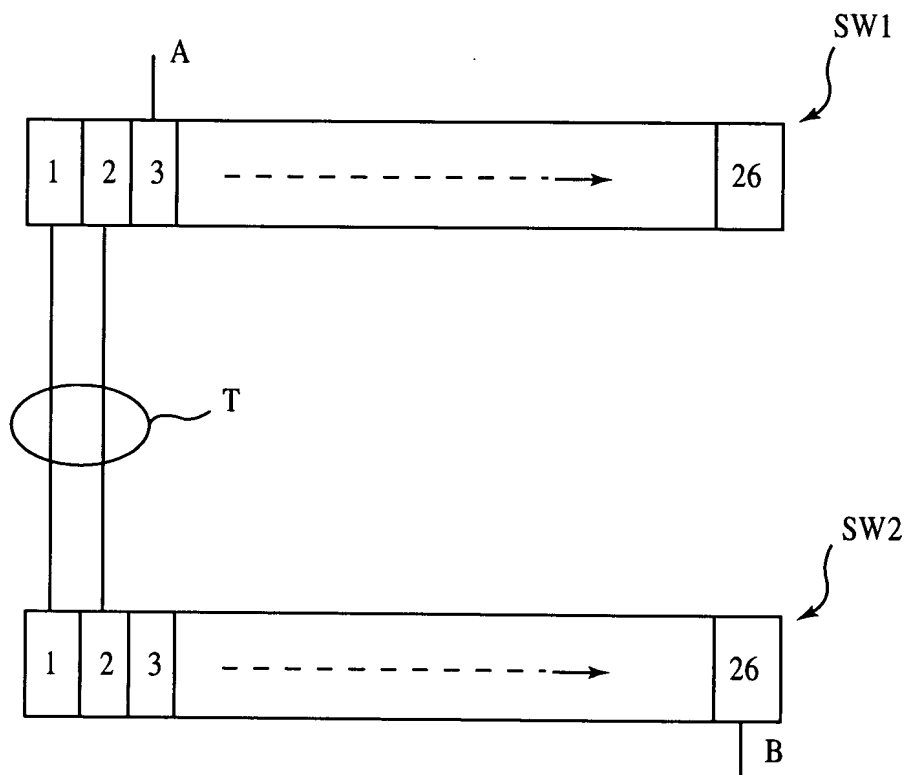


Fig.19

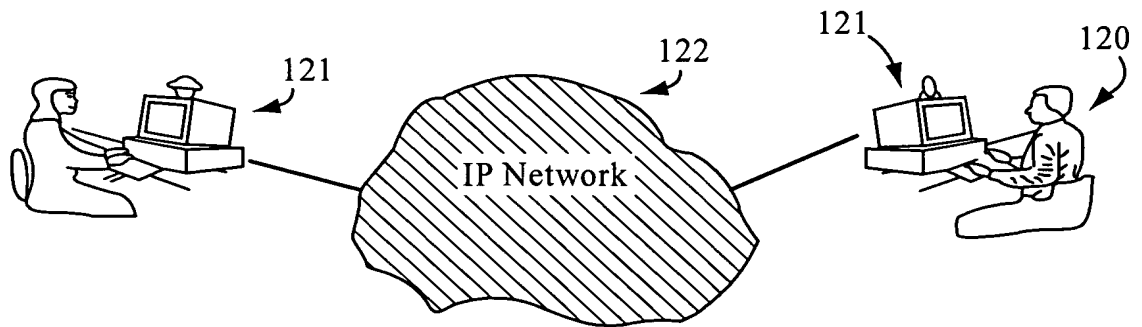
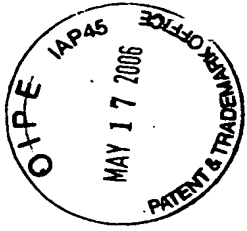


Fig.20

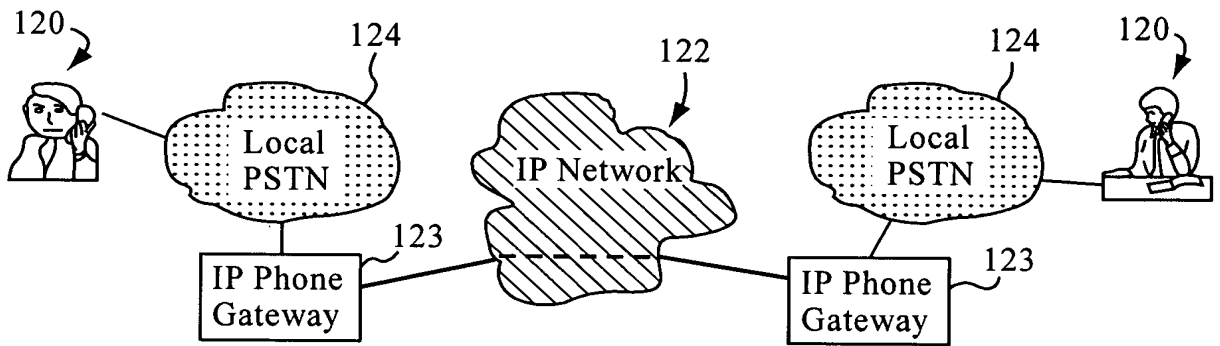
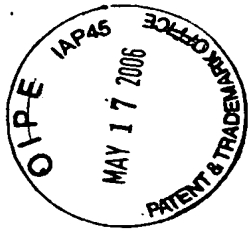


Fig.21

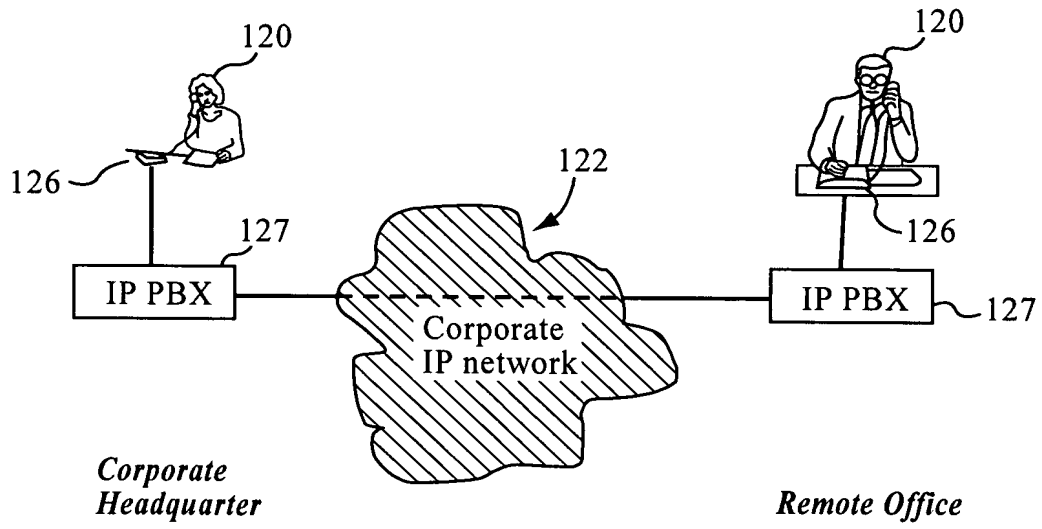
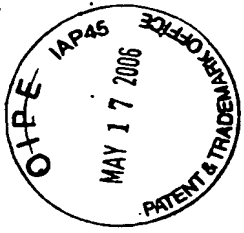


Fig.22

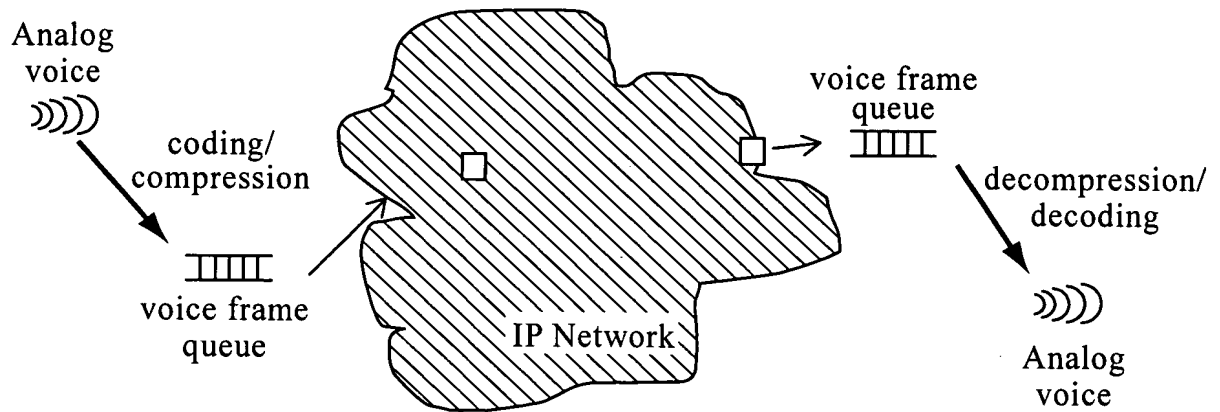
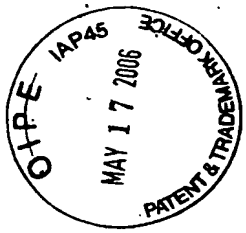


Fig.23

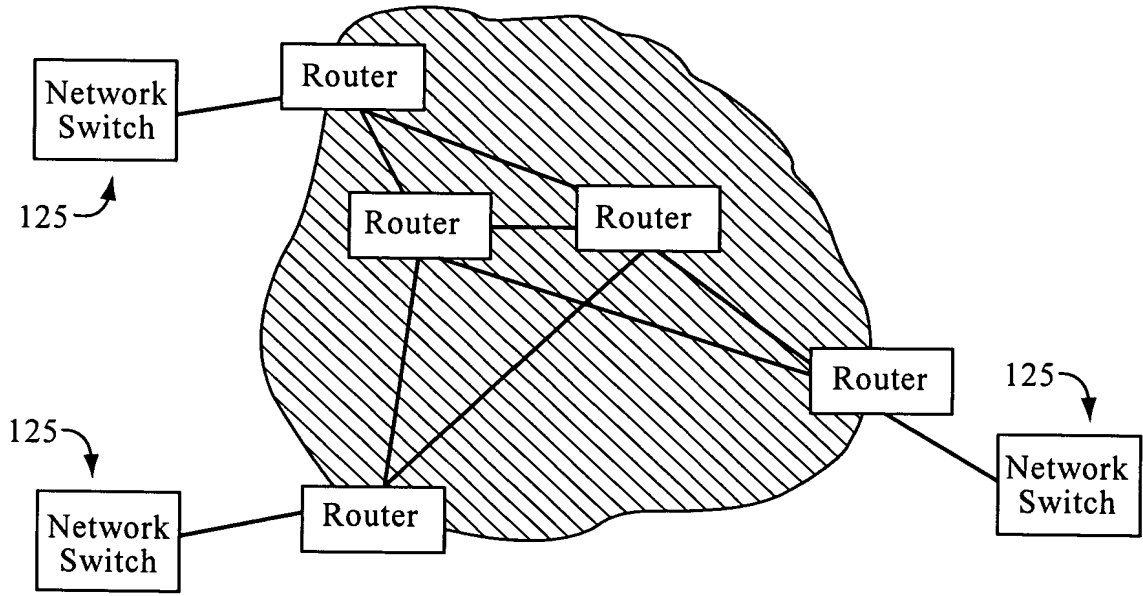
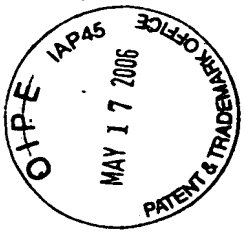


Fig.24

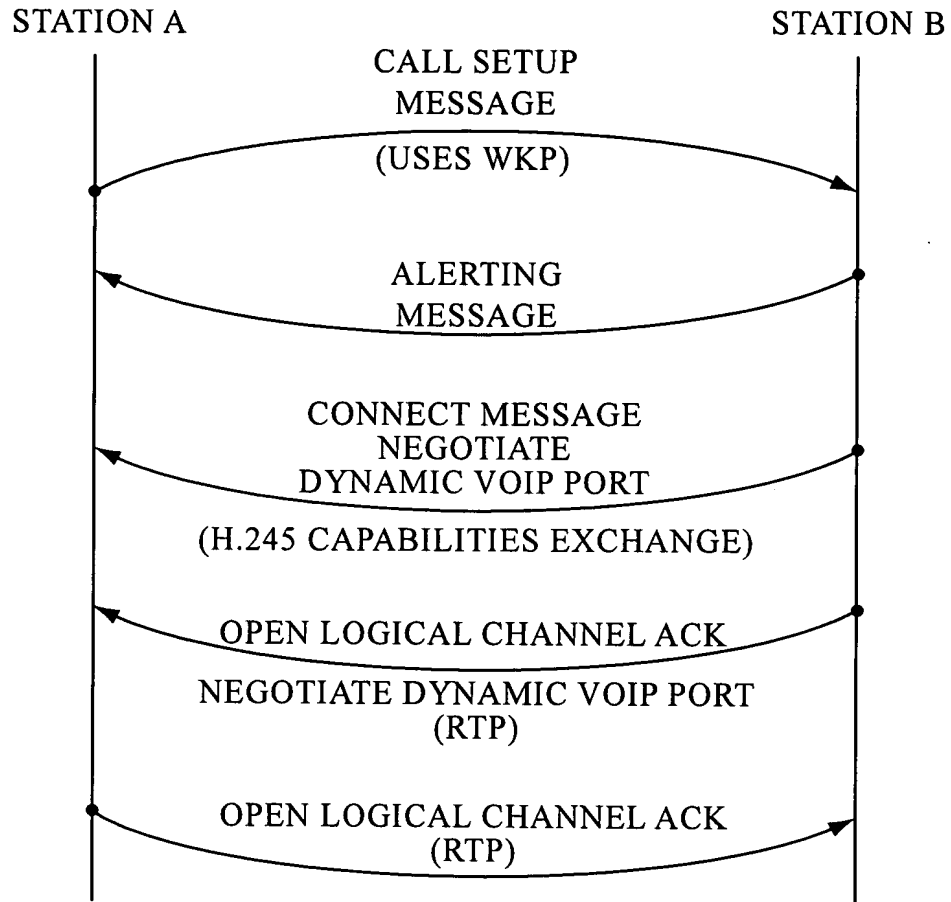


Fig.25

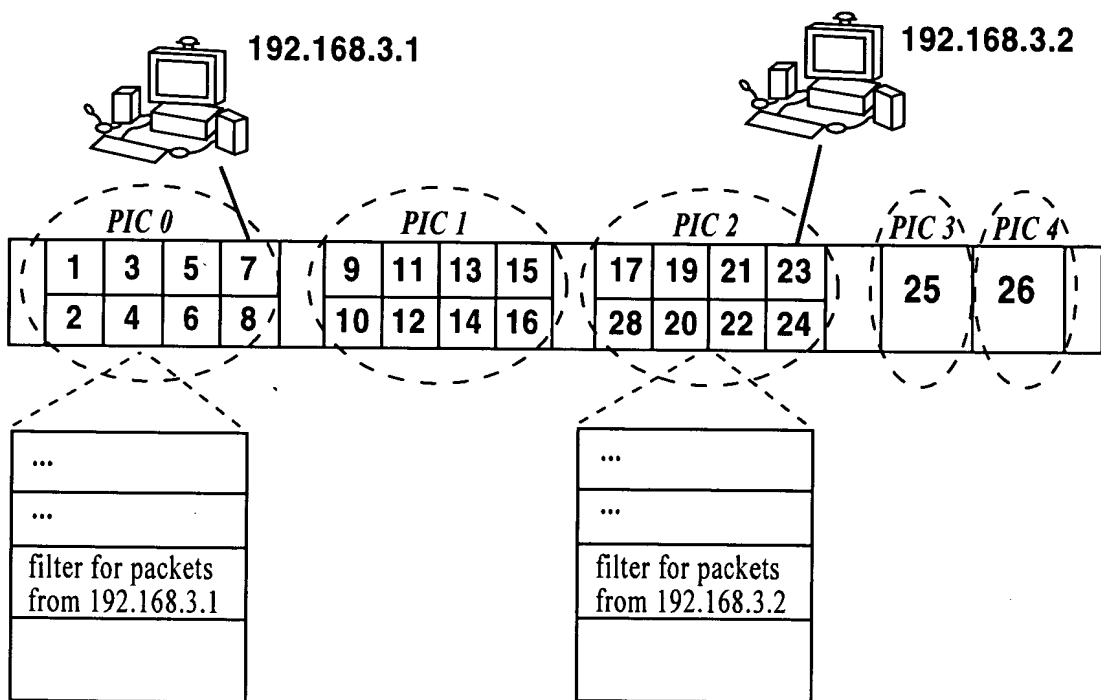
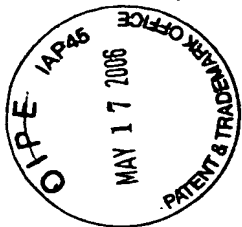


Fig.26

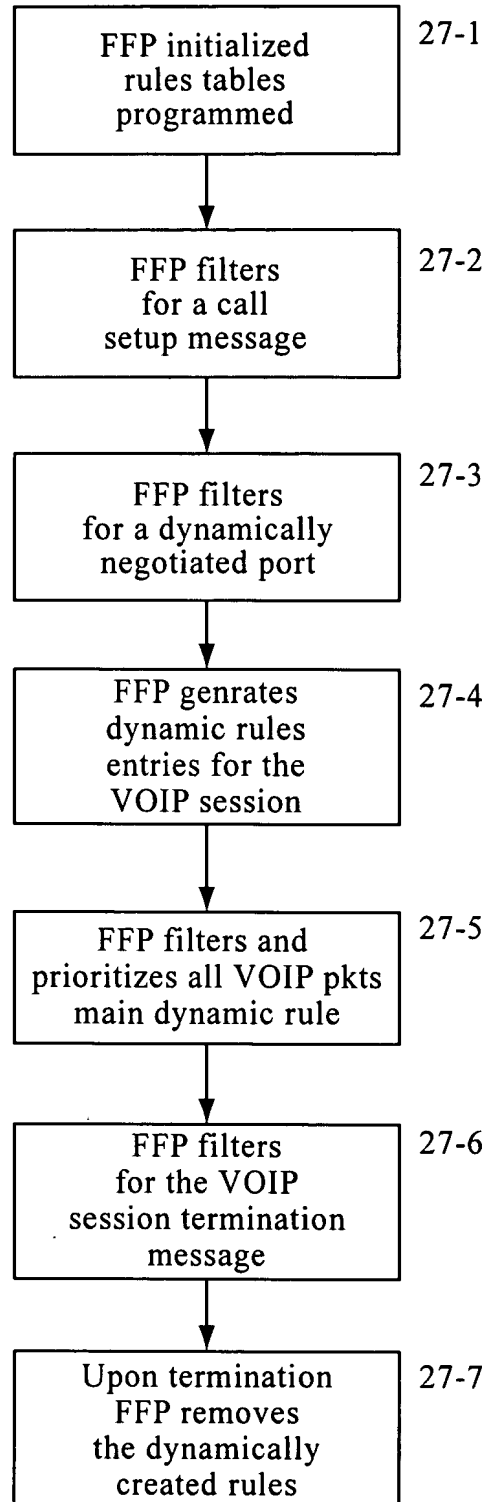


Fig.27